WHAT IS CLAIMED IS:

1.    A FIFO memory for use with read and write pointers and read and write clock signals, the FIFO memory comprising:

a write counter for updating the write pointer in accordance with the write clock signal;

a read counter for updating the read pointer in accordance with the read clock signal;

a memory connected to the write counter and the read counter and having a plurality of memory cells, the memory performing a write operation for writing data to a memory cell corresponding to the write pointer, and a read operation for reading data from a memory cell corresponding to the read pointer;

a full flag control circuit for indicating a memory full condition by generating a full flag synchronously with the write clock signal when the current read pointer and the next write pointer match; and

an empty flag control circuit for indicating a memory empty condition by generating an empty flag synchronously with the read clock signal when the current write pointer and the next read pointer match.

2.    The FIFO memory of claim 1, further comprising:

a first comparison circuit connected to the write counter and the read counter, for comparing the current read pointer and the next write pointer, and generating a first signal for generating the full flag in the full flag control circuit when the current read pointer and the next write pointer match; and

a second comparison circuit connected to the write counter and the read counter, for comparing the current

write pointer and the next read pointer, and generating a
second signal for generating an empty flag in the empty flag
control circuit when the current write pointer and the next
read pointer match.

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     3.    The FIFO memory of claim 2, further comprising:
    a third comparison circuit connected to the write
counter and the read counter, for comparing the current read
pointer and the current write pointer, and generating a

10    third signal to cancel either the full flag in the full flag
control circuit or cancel the empty flag in the empty flag
control circuit when the current read pointer and the
current write pointer do not match.

15     4.    The FIFO memory of claim 3, wherein the full flag
control circuit includes a first comparison result
determination circuit connected to the third comparison
circuit, for receiving the third signal synchronously with
the write clock signal, and the empty flag control circuit

20    includes a second comparison result determination circuit
connected to the third comparison circuit, for receiving the
third signal synchronously with the read clock signal.

     5.    The FIFO of claim 4, wherein at least one of the

25    first and second comparison result determination circuits
includes a flip-flop circuit having a data output terminal
for outputting a signal, and a reset input terminal to feed
back a signal delayed by a predetermined time, for
generating a pulse signal having a pulse width corresponding

30    to the predetermined delay time.

     6.    The FIFO memory of claim 5, wherein each clock
signal has an edge and an opposite edge and at least one of

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the first and second comparison result determination
circuits includes an initialization circuit connected to the
flip-flop circuit, for detecting the opposite edge of the
edge of the write clock signal or the read clock signal when
5   the flip-flop circuit receives a signal, and generating a
reset signal for resetting the flip-flop circuit.

7.   The FIFO memory of claim 2, wherein the full flag
control circuit includes a first comparison result
10  determination circuit connected to the first comparison
circuit, for receiving the first signal synchronously with
the write clock signal, the write clock signal being
controlled by the full flag, and the empty flag control
circuit includes a second comparison result determination
15  circuit connected to the second comparison circuit, for
receiving the second signal synchronously with the read
clock signal, the read clock signal being controlled by the
empty flag.

20      8.   The FIFO memory of claim 7, wherein at least one
of the first and second comparison result determination
circuits includes a flip-flop circuit having a data output
terminal for outputting a signal, and a reset input terminal
to feed back a signal delayed by a predetermined time, for
25  generating a pulse signal having a pulse width corresponding
to the predetermined delay time.

9.   The FIFO memory of claim 8, wherein each clock
signal has an edge and an opposite edge and at least one of
30  the first and second comparison result determination
circuits includes an initialization circuit connected to the
flip-flop circuit, for detecting the opposite edge of the
edge of the write clock signal or the read clock signal when

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the flip-flop circuit receives a signal, and generating a
reset signal for resetting the flip-flop circuit.

10.   The FIFO memory of claim 1, wherein the write
counter includes:
       a plurality of flip-flop circuits for generating a
current write pointer synchronously with the write clock
signal, the write clock signal being controlled by the full
flag; and
       a count-up logic circuit connected to the plurality of
flip-flop circuits, for incrementing the current write
pointer and generating a next write pointer.

11.   The FIFO memory of claim 1, wherein the read
counter includes:
       a plurality of flip-flop circuits for generating a
current read pointer synchronously with the read clock
signal, the read clock signal being controlled by the empty
flag; and
       a count-up logic circuit connected to the plurality of
flip-flop circuits, for incrementing the current read
pointer and generating a next read pointer.

12.   The FIFO memory of claim 1, wherein the memory
performs a write operation in response to the current write
pointer supplied from the write counter and performs a read
operation in response to the current read pointer supplied
from the read counter.

13.   The FIFO memory of claim 1, wherein the memory
receives beforehand a next write pointer supplied from the
write counter and performs a write operation synchronously
with the write clock signal, the write clock signal being

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controlled by the full flag, and receives beforehand a next read pointer supplied from the read counter and performs a read operation synchronously with the read clock signal, the read clock signal being controlled by the empty flag.

14.    The FIFO memory of claim 1, wherein the memory comprises:

a first shift register for sequentially selecting memory cells synchronously with the write clock signal, the write signal being controlled by the full flag;

a write circuit connected to the first shift register, for writing data to the memory cell selected by the first shift register;

a second shift register for sequentially selecting memory cells synchronously with the read clock signal, the read clock signal being controlled by the empty flag; and

a read circuit connected to the second shift register, for reading data from the memory cell selected by the second shift register.

15.    A FIFO memory for use with read and write pointers and read and write clock signals, the FIFO memory comprising:

a write counter for updating the write pointer in accordance with the write clock signal;

a read counter for updating the read pointer in accordance with the read clock signal;

a memory connected to the write counter and the read counter and having a plurality of memory cells, the memory performing a write operation for writing data to a memory cell corresponding to the write pointer, and a read operation for reading data from a memory cell corresponding to the read pointer;

a full flag control circuit for indicating a memory full condition by generating a full flag synchronously with the write clock signal when the current read pointer and the next write pointer match, and canceling the full flag

5      synchronously with the write clock signal when the current read pointer and the current write pointer do not match; and

an empty flag control circuit for indicating a memory empty condition by generating an empty flag synchronously with the read clock signal when the current write pointer

10     and the next read pointer match, and canceling the empty flag synchronously with the read clock signal when the current read pointer and the current write pointer do not match.

15          16.   A semiconductor device comprising:

a FIFO memory for use with read and write pointers and read and write clock signals, wherein the FIFO memory includes:

a write counter for updating the write pointer in

20     accordance with the write clock signal;

a read counter for updating the read pointer in accordance with the read clock signal;

a memory connected to the write counter and the read counter and having a plurality of memory cells, the

25     memory performing a write operation for writing data to a memory cell corresponding to the write pointer, and a read operation for reading data from a memory cell corresponding to the read pointer;

a full flag control circuit for indicating a

30     memory full condition by generating a full flag synchronously with the write clock signal when the current read pointer and the next write pointer match; and

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an empty flag control circuit for indicating a memory empty condition by generating an empty flag synchronously with the read clock signal when the current write pointer and the next read pointer match.

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17.  A semiconductor device comprising:

a FIFO memory for use with read and write pointers and read and write clock signals, wherein the FIFO memory includes:

10     a write counter for updating the write pointer in accordance with the write clock signal;

a read counter for updating the read pointer in accordance with the read clock signal;

a memory connected to the write counter and the

15  read counter and having a plurality of memory cells, the memory performing a write operation for writing data to a memory cell corresponding to the write pointer, and a read operation for reading data from a memory cell corresponding to the read pointer;

20     a full flag control circuit for indicating a memory full condition by generating a full flag synchronously with the write clock signal when the current read pointer and the next write pointer match, and canceling the full flag synchronously with the write clock signal when

25  the current read pointer and the current write pointer do not match; and

an empty flag control circuit for indicating a memory empty condition by generating an empty flag synchronously with the read clock signal when the current

30  write pointer and the next read pointer match, and canceling the empty flag synchronously with the read clock signal when the current read pointer and the current write pointer do not match.

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